	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Errors
1	IS&R	L1	0	("microprocessorsameaddressingadjunitsamedataadjpathsamecache").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/05/04 10:11			
2	BRS	L2	3	microprocessor same addressing adj unit same data adj path same cache	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/05/04 10:14			
3	BRS	L3	21	multi-precision adj execution	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/05/04 10:18			
4	BRS	L4	18	3 not 2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/05/04 10:14			
5	BRS	L5	3	4 and (addressing adj unit same data adj path same cache)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/05/04 10:15			

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Errors
6	BRS	L6	12	4 and addressing adj unit	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/05/04 10:15			
7	BRS	L7	9	6 not 5	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/05/04 10:15			
8	BRS	L9	52	group adj floating adj point	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/05/04 10:20			
9	BRS	L10	49	9 not 5	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/05/04 10:32			
10	BRS	L11	46	10 not 2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/05/04 10:21			

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Errors
11	BRS	L12	37	11 not 7	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/05/04 11:36			
12	BRS	L13	2	12 and (partitioned adj (file or register or data))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/05/04 10:32			
13	BRS	L14	0	cantenated adj result	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/05/04 10:32			
14	BRS	L16	3585643	"23" not 5	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/05/04 10:33			
15	BRS	L17	20	15 not 5	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/05/04 10:33			

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Errors
16	BRS	L18	17	17 not 2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/05/04 10:33			
17	BRS	L19	8	18 not 7	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/05/04 10:33			
18	BRS	L15	23	catenated adj result	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/05/04 11:16			
19	BRS	L8	25	multi-precision near3 unit	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/05/04 11:18			

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Errors
20	IS&R	L20	116	(("4,785,393") or ("4.814,976") or ("5,031,135") or ("5,280,598") or ("5,481,686") or ("5.487,024") or ("5,600,814") or ("5,740,093") or ("5,742840") or ("5,768,546") or ("5,898,849") or ("5,996,057") or ("6,041,404") or ("6,052,769") or ("6,173,393") or ("6,275,834") or ("6,295,599") or ("4,025,772") or ("4489393") or ("4,701,875") or ("4,727,505") or ("4,876,660") or ("4,893,267") or ("4,956,801") or ("4,969,118") or ("4,975,868") or ("5,032,865") or ("5,157,388") or ("5,201,056") or ("5,268,855") or ("5,268,995") or ("5,408,581") or ("5,423,051") or ("5,426,600") or ("5,500,811") or ("5,557,724") or ("5,588,152") or ("5,592,405") or ("5,640,543") or ("5,642,306") or ("5,666,298") or ("5,669,010") or ("5,673,407") or ("5,675,526") or ("5,680,338") or ("5,721,892") or ("5,734,874") or ("5,757,432") or ("5,758,176") or ("5,802,336") or ("5,809,292") or ("5,818,739") or ("5,825,677") or ("5,835,782") or ("5,886,732") or ("5,922,066") or ("5,983,257") or ("6,016,538") or ("6,092,094") or ("6,401,194")).PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/05/04 11:41			

21	IS&R	L21	1231	((712/221,222) or (708/620,523,524)).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/05/04 11:42			
22	BRS	L22	3429	20 0r 21	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/05/04 11:43			

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Errors
23	BRS	L23	3429	22 or 21	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/05/04 11:43			
24	BRS	L24	1331	20 or 21	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/05/04 11:43			
25	BRS	L25	16	20 and 21	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/05/04 11:43			

Terms used **floating point operation** and **bus** and **microprocessor** and **register** and **partioned field** and **catenated** and **multi precision** and **data path** and **interface** and **programmable** and **group**

Found **11,132** of **154,226**

Sort results by relevance

Display results expanded form

Save results to a Binder

Search Tips

Open results in a new window

Try an Advanced Search

Try this search in The ACM Guide

Results 1 - 20 of 200 Result page: **1** 2 3 4 5 6 7 8 9 10 next

Best 200 shown

Relevance scale

1 The Clipper processor: instruction set architecture and implementation

W. Hollingsworth, H. Sachs, A. J. Smith

February 1989 **Communications of the ACM**, Volume 32 Issue 2

Full text available: pdf(4.67 MB) Additional Information: full citation, abstract, references, citings, index terms, review

Intergraph's CLIPPER microprocessor is a high performance, three chip module that implements a new instruction set architecture designed for convenient programmability, broad functionality, and easy future expansion.

2 Formal verification in hardware design: a survey

Christoph Kern, Mark R. Greenstreet

April 1999 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 4 Issue 2

Full text available: pdf(411.53 KB) Additional Information: full citation, abstract, references, citings, index terms

In recent years, formal methods have emerged as an alternative approach to ensuring the quality and correctness of hardware designs, overcoming some of the limitations of traditional validation techniques such as simulation and testing. There are two main aspects to the application of formal methods in a design process: the formal framework used to specify desired properties of a design and the verification techniques and tools used to reason about the relationship between a spec ...

Keywords: case studies, formal methods, formal verification, hardware verification, language containment, model checking, survey, theorem proving

3 A survey of commercial parallel processors

Edward Gehringer, Janne Abullarade, Michael H. Gulyn

September 1988 **ACM SIGARCH Computer Architecture News**, Volume 16 Issue 4

Full text available: pdf(2.96 MB) Additional Information: full citation, abstract, citings, index terms

This paper compares eight commercial parallel processors along several dimensions. The processors include four shared-bus multiprocessors (the Encore Multimax, the Sequent Balance system, the Alliant FX series, and the ELXSI System 6400) and four network multiprocessors (the BBN Butterfly, the NCUBE, the Intel iPSC/2, and the FPS T Series). The paper contrasts the computers from the standpoint of interconnection structures, memory configurations, and interprocessor communication. Also, the share ...

4 A decade of reconfigurable computing: a visionary retrospective
R. Hartenstein
March 2001 **Proceedings of the conference on Design, automation and test in Europe**
Full text available: pdf(768.00 KB) Additional Information: full citation, references, citings, index terms

5 Hardware speedups in long integer multiplication
M. Shand, P. Bertin, J. Vuillemin
March 1991 **ACM SIGARCH Computer Architecture News**, Volume 19 Issue 1
Full text available: pdf(772.85 KB) Additional Information: full citation, abstract, citings, index terms

We present various experiments in Hardware/Software design tradeoffs met in speeding up long integer multiplications. This work spans over a year, with more than 12 different hardware designs tested and measured.To implement these designs, we rely on our PAM (for *Programmable Active Memory*, see [BRV]) technology which provides us with a 50 millisecond turn-around time silicon foundry for implementing up to 50K gate logic designs fully equipped with fast local RAM and host bus interface.Fi ...

6 Simulation hierarchy for microprocessor design
Will Sherwood
February 1977 **Proceedings of the Symposium on Design Automation and Microprocessors**
Full text available: pdf(434.73 KB) Additional Information: full citation, abstract, references, index terms

There are many levels of abstraction through which a designer passes when implementing a microprocessor chip set or system. He usually begins by configuring the application for the microprocessor, bus, and peripherals (memory, etc.). Section at a time, he expands the system components into a Register Transfer level diagram, followed by a detailed chip or gate description. This paper will show how a hierarchical simulator aids each phase in the design by modeling elements at all levels from ...

Keywords: Computer aided design, Gate level, Hierarchical simulation, Microprocessors, PMS, Register transfer level, Software breadboard

7 Hardware speedups in long integer multiplication
M. Shand, P. Bertin, J. Vuillemin
May 1990 **Proceedings of the second annual ACM symposium on Parallel algorithms and architectures**
Full text available: pdf(939.04 KB) Additional Information: full citation, references, citings, index terms

8 The white dwarf: a high-performance application-specific processor
A. Wolfe, M. Breternitz, C. Stephens, A. L. Ting, D. B. Kirk, R. P. Bianchini, J. P. Shen
May 1988 **ACM SIGARCH Computer Architecture News , Proceedings of the 15th Annual International Symposium on Computer architecture**, Volume 16 Issue 2
Full text available: pdf(1.40 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents the design and implementation of a high-performance special-purpose processor, called The White Dwarf, for accelerating finite element analysis algorithms. The White Dwarf CPU contains two Am29325 32-bit floating-point processors and one Am29332 32-bit ALU, and employs a wide-instruction word architecture in which the application algorithm is directly implemented in microcode. The entire system is VME-bus compatible and interfaces with a SUN 31160 host. The syste ...

9 Survey of commercial parallel machines
Gowri Ramanathan, Joel Oren

June 1993 **ACM SIGARCH Computer Architecture News**, Volume 21 Issue 3

Full text available: pdf(1.64 MB) Additional Information: full citation, abstract, citings, index terms

We have presented in this paper the survey of the parallel machines that are marketed today. The survey includes the latest machines available from Kendell Square Research, Thinking Machines Corporation, MasPar Computer Corporation, NCUBE Corporation, Sequent Computer Systems and Parsytec. We have provided the topology, architecture, cache coherence, synchronization and performance in MFLOPs for each of the machines subject to the availability of information.

10 Mark IIIfp hypercube concurrent processor architecture

J. Tuazon, J. Peterson, M. Pniel

January 1988 **Proceedings of the third conference on Hypercube concurrent computers and applications: Architecture, software, computer systems, and general issues - Volume 1**

Full text available: pdf(1.02 MB) Additional Information: full citation, abstract, references, citings, index terms

The Mark IIIfp Hypercube is a new generation of hypercube concurrent processor system developed at JPL/Caltech, with peak performance of 5 Mips, 14 Mflops per node, and a peak communication rate of 6 Mbytes per second. Each node utilizes two Motorola MC68020 microprocessors, an MC68882 scalar floating- point coprocessor, and a Weitek 8000 floating-point chip set. One of the MC68020 processors serves as the application and computational processor, the other is dedicated to communication. The ...

11 Computer structures: What have we learned from the PDP-11?

Gordon Bell, William D. Strecker

January 1976 **ACM SIGARCH Computer Architecture News , Proceedings of the 3rd annual symposium on Computer architecture**, Volume 4 Issue 4

Full text available: pdf(893.62 KB) Additional Information: full citation, abstract, references, citings, index terms

Over the PDP-11'S six year life about 20,000 specimens have been built based on 10 species (models). Although range was a design goal, it was unquantified; the actual range has exceeded expectations (500:1 in memory size and system price). The range has stressed the basic mini(mal) computer architecture along all dimensions. The main PMS structure, i.e. the UNIBUS, has been adopted as a de facto standard of interconnection for many micro and minicomputer systems. The architectural experienc ...

12 A 50-Gb/s IP router

Craig Partridge, Philip P. Carvey, Ed Burgess, Isidro Castineyra, Tom Clarke, Lise Graham, Michael Hathaway, Phil Herman, Allen King, Steve Kohalmi, Tracy Ma, John Mcallen, Trevor Mendez, Walter C. Milliken, Ronald Pettyjohn, John Rokosz, Joshua Seeger, Michael Sollins, Steve Storch, Benjamin Tober, Gregory D. Troxel

June 1998 **IEEE/ACM Transactions on Networking (TON)**, Volume 6 Issue 3

Full text available: pdf(133.28 KB) Additional Information: full citation, references, citings, index terms, review

Keywords: data communications, internetworking, packet switching, routing

13 Exploiting parallel microprocessor microarchitectures with a compiler code generator

W. W. Hwu, P. P. Chang

May 1988 **ACM SIGARCH Computer Architecture News , Proceedings of the 15th Annual International Symposium on Computer architecture**, Volume 16 Issue 2

Full text available: pdf(890.51 KB) Additional Information: full citation, abstract, references, citings, index terms

With advances in VLSI technology, microprocessor designers can provide more microarchitectural parallelism to increase performance. We have identified four major forms

of such parallelism: multiple microoperations issued per cycle, multiple result distribution buses, multiple execution units, and pipelined execution units. The experiments reported in this paper address two important issues: The effects of these forms and the appropriate balance among them. A central microar ...

14 System architectures for computer music

John W. Gordon

June 1985 **ACM Computing Surveys (CSUR)**, Volume 17 Issue 2

Full text available: pdf(4.61 MB) Additional Information: full citation, abstract, references, citings, index terms, review

Computer music is a relatively new field. While a large proportion of the public is aware of computer music in one form or another, there seems to be a need for a better understanding of its capabilities and limitations in terms of synthesis, performance, and recording hardware. This article addresses that need by surveying and discussing the architecture of existing computer music systems. System requirements vary according to what the system will be used for. Common uses for co ...

15 Computer structures: what have we learned from the PDP-11?

Gordon Bell, William D. Strecker

August 1998 **25 years of the international symposia on Computer architecture (selected papers)**

Full text available: pdf(1.14 MB) Additional Information: full citation, references, index terms

16 A parallel computer based on cube connected cycles for wafer scale integration

Moon Jung Chung, Edward J. Toy, Aarti Gupta

November 1999 **Proceedings of 1986 ACM Fall joint computer conference**

Full text available: pdf(1.15 MB) Additional Information: full citation, references, index terms

Keywords: VLSI, computer architecture, cube connected cycles, parallel processing, wafer scale integration

17 Warp architecture and implementation

M. Annaratone, E. Arnould, T. Gross, H. T. Kung, M. S. Lam

June 1986 **ACM SIGARCH Computer Architecture News , Proceedings of the 13th annual international symposium on Computer architecture**, Volume 14 Issue 2

Full text available: pdf(1.17 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper describes the scan line array processor (SLAP), a new architecture designed for high-performance yet low-cost image computation. A SLAP is a SIMD linear array of processors, and hence is easy to build and scales well with VLSI technology; yet appropriate special features and programming techniques make it efficient for a surprisingly wide variety of low and medium level computer vision tasks. We describe the basic SLAP concept and some of its variants, discuss a particular planne ...

18 MIPS: A microprocessor architecture

John Hennessy, Norman Jouppi, Steven Przybylski, Christopher Rowen, Thomas Gross, Forest Baskett, John Gill

October 1982 **ACM SIGMICRO Newsletter , Proceedings of the 15th annual workshop on Microprogramming**, Volume 13 Issue 4

Full text available: pdf(538.60 KB) Additional Information: full citation, abstract, references, citings, index terms

MIPS is a new single chip VLSI microprocessor. It attempts to achieve high performance with the use of a simplified instruction set, similar to those found in microengines. The

processor is a fast pipelined engine without pipeline interlocks. Software solutions to several traditional hardware problems, such as providing pipeline interlocks, are used.

19 Integration of message passing and shared memory in the Stanford FLASH multiprocessor

John Heinlein, Kourosh Gharachorloo, Scott Dresser, Anoop Gupta

November 1994 **Proceedings of the sixth international conference on Architectural support for programming languages and operating systems**, Volume 29 , 28 Issue 11 , 5

Full text available: pdf(1.80 MB) Additional Information: full citation, abstract, references, citings, index terms

The advantages of using message passing over shared memory for certain types of communication and synchronization have provided an incentive to integrate both models within a single architecture. A key goal of the FLASH (FLexible Architecture for SHared memory) project at Stanford is to achieve this integration while maintaining a simple and efficient design. This paper presents the hardware and software mechanisms in FLASH to support various message passing protocols. We achieve low overhe ...

20 Dissertation Abstracts in Computer Graphics

January 1992 **ACM SIGGRAPH Computer Graphics**, Volume 26 Issue 1

Full text available: pdf(2.53 MB) Additional Information: full citation

Results 1 - 20 of 200 Result page: **1** 2 3 4 5 6 7 8 9 10 next